CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

1. An output stage for a line driver, comprising:

a first amplifier comprising a series combination of a first semiconductor device and a second semiconductor device;

a second amplifier comprising a series combination of a third semiconductor device and a fourth semiconductor device;

a first integrated back-matching resistor network interposed between the first and the second semiconductor devices; and

a second integrated back-matching resistor network interposed between the third and the fourth semiconductor devices.

2. The line driver of claim 1, wherein the first integrated back-matching resistor network comprises a series combination of integrated resistors having an additive resistance selected to match an expected load input impedance.

3. The line driver of claim 2, wherein the second integrated back-matching resistor network comprises a series combination of integrated resistors having an additive resistance selected to emulate an expected line input impedance.

4. The line driver of claim 3, wherein the series combination of integrated resistors selected to match the expected load input impedance are configured in parallel with the series combination of integrated resistors selected to emulate the expected line input impedance.

5. The line driver of claim 4, wherein a supply voltage applied to a source node of the first and second semiconductor devices of the first and second amplifiers respectively, is increased to a voltage level exceeding the maximum drain-source voltage for the semiconductor device technology associated with the first and second semiconductor devices, resulting in an available maximum power increase at the line driver output.

6. The line driver of claim 5, wherein the available maximum power increase at the line driver output is realizable without increasing the maximum current in the line driver output stage.

7. The line driver of claim 5, wherein the first, second, third, and fourth semiconductor devices are standard CMOS devices.

8. The line driver of claim 7, wherein the first and third semiconductor devices are PMOS transistors.

9. The line driver of claim 7, wherein the second and fourth semiconductor devices are NMOS transistors.

10. The line driver of claim 7, wherein the standard CMOS devices have a maximum drain-source voltage of approximately 5 Volts.

11. The line driver of claim 10, wherein the power supply maximum voltage is approximately 20/3 Volts.

12. The line driver of claim 11, wherein the effective signal swing across a load is approximately 10/3 Volts.

13. The line driver of claim 11, wherein the effective power gain available at the output of the line driver is greater than approximately 2.5 dB larger then the effective power gain of a conventional line driver.

14. The line driver of claim 13, wherein the effective power gain available at the output of the line driver is approximately 3.0 dB larger then the effective power gain of a conventional line driver.

15. An output stage for a line driver, comprising:

a first amplifier comprising a series combination of a first semiconductor device and a second semiconductor device;

a second amplifier comprising a series combination of a third semiconductor device and a fourth semiconductor device;

a first integrated back-matching resistor interposed between the first and the second semiconductor devices and a first line driver output node;

a second integrated back-matching resistor interposed between the third and the fourth semiconductor devices and a second line driver output node;

a first supply voltage protective semiconductor device interposed in series between the first semiconductor device and the first integrated back-matching resistor;

a second supply voltage protective semiconductor device interposed in series between the first integrated back-matching resistor and the second semiconductor device;

a third supply voltage protective semiconductor device interposed in series between the third semiconductor device and the second integrated back-matching resistor; and

a fourth supply voltage protective semiconductor device interposed in series between the second integrated back-matching resistor and the fourth semiconductor device.

16. The line driver of claim 15, wherein the sum of the resistance values of the first and the second integrated back-matching resistors is selected to match an expected load input impedance.

17. The line driver of claim 15, wherein the first and second supply voltage protective semiconductor devices comprise at least one source follower.

18. The line driver of claim 15, wherein the first and second supply voltage protective semiconductor devices protect only a respective semiconductor device that is idle.

19. The line driver of claim 16, wherein the first and second integrated back-matching resistors have a resistance of approximately the same value.

20. The line driver of claim 19, wherein a supply voltage is increased to a voltage level exceeding the maximum drain-source voltage for the semiconductor device technology associated with the first, second, third, and fourth semiconductor devices, resulting in an available maximum power increase at the line driver output.

21. The line driver of claim 20, wherein the available maximum power increase at the line driver output is realizable without increasing the maximum current in the line driver output stage.

22. The line driver of claim 21, wherein the power supply maximum voltage is approximately twice the maximum drain-source voltage of the semiconductor device technology of the first, second, third, and fourth semiconductor devices.

23. The line driver of claim 15, wherein the first, second, third, and fourth semiconductor devices are standard CMOS devices.

24. The line driver of claim 23, wherein the standard CMOS devices have a maximum drain-source voltage of approximately 5 Volts.

25. The line driver of claim 24, wherein the power supply maximum voltage is approximately 10 Volts.

26. The line driver of claim 25, wherein the first and third semiconductor devices are PMOS transistors.

27. The line driver of claim 25, wherein the second and fourth semiconductor devices are NMOS transistors.

28. The line driver of claim 25, wherein the first and third supply voltage protective semiconductor devices are PMOS transistors.

29. The line driver of claim 25, wherein the second and fourth supply voltage protective semiconductor devices are NMOS transistors.

30. The line driver of claim 25, wherein the effective signal swing across a load is approximately equivalent to the full power supply voltage range.

31. The line driver of claim 25, wherein the effective power gain available at the output of the line driver is approximately 6.0 dB larger then the effective power gain of a conventional line driver.

32. An output stage for a line driver, comprising:

a first amplifier comprising a series combination of a first semiconductor device, a first semiconductor protective device, a second semiconductor device, and a second semiconductor protective device, wherein the first and second semiconductor protective devices are interposed between the first semiconductor device and the second semiconductor devices;

a second amplifier comprising a series combination of a third semiconductor device, a third semiconductor protective device, a fourth semiconductor device, and a fourth semiconductor protective device, wherein the third and fourth semiconductor protective devices are interposed between the third semiconductor device and the fourth semiconductor devices;

a first integrated back-matching resistor network interposed between the first semiconductor protective device and a first pole of a transformer;

a second integrated back-matching resistor network interposed between the first pole of the transformer and the second semiconductor protective device;

a third integrated back-matching resistor network interposed between the third semiconductor protective device and a second pole of the transformer; and

a fourth integrated back-matching resistor network interposed between the second pole of the transformer and the fourth semiconductor protective device.

33. The line driver of claim 32, wherein the first, second, third, and fourth integrated back-matching resistor networks comprise a combination of integrated resistors having a resistance selected to match an expected load input impedance.

34. The line driver of claim 32, further comprising:

a first integrated resistor having a resistance selected to emulate an expected line input impedance interposed between the first and the second integrated back-matching resistor networks; and

a second integrated resistor having a resistance selected to emulate an expected line input impedance interposed between the third and the fourth integrated back-matching resistor networks.

35. The line driver of claim 32, wherein a supply voltage applied to a source node of the first and third semiconductor devices is increased to a voltage level exceeding the maximum drain-source voltage for the semiconductor device technology associated with the first, second, third, and fourth semiconductor devices, resulting in an available maximum power increase at the line driver output.

36. The line driver of claim 35, wherein the available maximum power increase at the line driver output is realizable without increasing the maximum current in the line driver output stage.

37. The line driver of claim 36, wherein the first, second, third, and fourth semiconductor devices are standard CMOS devices.

38. The line driver of claim 37, wherein the standard CMOS devices have a maximum drain-source voltage of approximately 5 Volts.

39. The line driver of claim 37, wherein the power supply maximum voltage is approximately 40/3 Volts.

40. The line driver of claim 37, wherein the first and third semiconductor devices are PMOS transistors.

41. The line driver of claim 37, wherein the second and fourth semiconductor devices are NMOS transistors.

42. The line driver of claim 37, wherein the first and third supply voltage protective semiconductor devices are PMOS transistors.

43. The line driver of claim 37, wherein the second and fourth supply voltage protective semiconductor devices are NMOS transistors.

44. The line driver of claim 39, wherein the effective signal swing across a load is approximately 20/3 Volts.

45. The line driver of claim 39, wherein the effective power gain available at the output of the line driver is greater than approximately 8.5 dB larger then the effective power gain of a conventional line driver.

46. The line driver of claim 39, wherein the effective power gain available at the output of the line driver is approximately 9.0 dB larger then the effective power gain of a conventional line driver.

47. An integrated circuit line driver, comprising:

means for increasing the effective output signal swing to at least a voltage level that exceeds the maximum drain-source voltage of the integrated circuit technology.

48. The line driver of claim 47, wherein the means for increasing the effective output signal swing is accomplished with an integrated resistor network.

49. The line driver of claim 47, wherein the means for increasing the effective output signal swing is accomplished with a combination of protective semiconductor devices and a plurality of integrated back-matching resistors.

50. The line driver of claim 47, wherein the protective semiconductor devices comprise at least one source follower.

51. The line driver of claim 49 wherein the protective semiconductor devices protect a semiconductor device that is idle.

52. A transmission unit, comprising:

a line driver having an output stage, wherein the output stage is configured to transmit a signal having a peak-to-peak voltage swing that exceeds the maximum drain-source voltage of the integrated circuit technology used to implement the line driver.

53. A communications system, comprising:

a transmission unit having an integrated line driver, the integrated line driver having an output stage, wherein the output stage is configured to transmit a signal having a peak-to-peak voltage swing that exceeds the maximum drain-source voltage of the integrated circuit technology used to implement the line driver.

54. A method of increasing the available signal transmit power on a transmission line, comprising:

applying a transmit signal to an input stage of an integrated line driver;

amplifying the transmit signal such that the output signal swing exceeds the maximum drain-source voltage of the integrated circuit technology used to implement an at least one amplifier in an integrated line driver output stage; and

applying the amplified transmit signal via an integrated resistor network to the transmission line.

55. The method of claim 54, wherein the integrated resistor network comprises:

a parallel combination of a first resistor branch comprising an at least balanced pair of integrated resistors selected to match an expected load impedance.

56. The method of claim 54, wherein the integrated resistor network comprises:

a pair of integrated back-matching resistors selected such that the sum of their resistance values approximates an expected load impedance, wherein each of the integrated back-matching resistors supplies half of the available signal transmit power to a load.

57. The method of claim 54, wherein the step of amplifying the transmit signal is accomplished by adding a plurality of protective semiconductor devices, wherein each of the plurality of protective semiconductor devices protects a corresponding semiconductor device when the corresponding semiconductor device is idle.

58. The method of claim 57, wherein each of the plurality of protective semiconductor devices comprise at least one source follower.